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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/799,780	03/15/2004	Satoshi Inaba	250386US2	8643

22850 7590 11/10/2005

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EXAMINER	
HO, TU TU V	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 11/10/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)
	10/799,780	INABA ET AL.
	Examiner	Art Unit
	Tu-Tu Ho	2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 November 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) *3 and 13-20* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,2 and 4-12* is/are rejected.

7)☒ Claim(s) *2* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 March 2004* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Oath/Declaration

1. The oath/declaration filed on 07/27/2004 is acceptable.

Election/ Restriction

2. Applicant's election with traverse of Species I, claims 1, 2, and 4-12, in the reply filed on 11/01/2005, is acknowledged. The traversal is on the ground(s) that a search and examination of all the species will not pose a serious burden. This is not found persuasive because a search and examination of all the species will pose a serious burden.

The requirement is still deemed proper and is therefore made FINAL.

3. Claim 20 is withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on 06/30/2005. Claims 3 and 13-19 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected species, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 11/01/2005, as noted above.

Drawings

4. **Figure 29** should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR

1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.121(d)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

5. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "the respective loop-shaped gate electrode regions have same lengths on the device region and a device isolation region except contact regions between wiring portions and the gate electrode regions" of **claim 8** must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will

be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

6. **Claim 2** is objected to because of the following informalities: claim 2 recites: "part of which are", which is not clear because it is not clear whether the part refers to a loop-shaped gate electrode region or to two or more parts of two or more loop-shaped gate electrode regions or to two or more loop-shaped gate electrode regions. If the part refers to two or more parts of two or more loop-shaped gate electrode regions or to two or more loop-shaped gate electrode regions then the limitation does not carry any patentable weight because a device comprising a device region where each of a plurality of source regions and each of a plurality of drain regions of transistors are alternately included and a plurality of loop-shaped gate electrode regions of the transistors which are formed on the device region, then two or more loop-shaped gate electrode regions are inherently disposed onto two positions between the source regions and the drain regions. Therefore "part of which are" is interpreted to be "portions of each loop-shaped gate electrode region of the plurality of loop-shaped gate electrode regions are" for examination purposes. Appropriate correction is required.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter that the applicant regards as his invention.

7. **Claims 8-12** are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 8 recites "the respective loop-shaped gate electrode regions" in "the respective loop-shaped gate electrode regions have same lengths on the device region and a device isolation region except contact regions between wiring portions and the gate electrode regions" wherein "the respective loop-shaped gate electrode regions" does not have a proper antecedent basis. Furthermore, it is not clear what sections of the loop-shaped gate electrode region have the same length and/or with respect to what exception.

Claim 9 recites: "the first and second conductivity type transistors" which lack an antecedent basis.

Claims 10-12 depend from rejected claims 9 and include all limitations of claim 9 thereby rendering these claims indefinite.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in
> (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or
> (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. **Claims 1 and 4-6** are rejected under 35 U.S.C. 102(e) as being anticipated by Hebert U.S. Patent 6,888,207 (the '207 reference).

The '207 reference discloses in the figures, particularly Fig. 3, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device, comprising:

a first transistor (left transistor) including a source region (352 or 352/353, Fig. 3), a drain region (363) provided in the same device region as the source region, and a loop-shaped gate electrode region (355, column 6, last paragraph); and

a second transistor (right transistor) sharing, with the first transistor, the loop-shaped gate electrode region and (the source region or) the drain region.

Referring to **claim 4**, the reference further discloses that the drain region (363) is formed in a region surrounded by the loop-shaped gate electrode region.

Referring to **claim 5**, the reference further discloses that an electrically independent drain region (363) is formed in a region surrounded by the loop-shaped electrode region.

Referring to **claim 6**, the reference further discloses that the source region (352 or 352/353) is formed outside a region surrounded by the loop-shaped gate electrode region.

9. **Claim 2** is rejected under 35 U.S.C. 102(b) as being anticipated by Kumagai U.S. Patent 6,057,568 (the '568 reference).

The '207 reference discloses in the figures, particularly Figs. 4's, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 2**, the reference discloses a semiconductor device, comprising:

a device region where each of a plurality of source regions (106a, 107a, Figs. 4, from first row and third row) and each of a plurality of drain regions (106a, 107a, Figs. 4, from second row and fourth row) of transistors are alternately included; and

a plurality of loop-shaped gate electrode regions (108a, 109a, column 5, lines 30-67) of the transistors which are formed on the device region and portions of each loop-shaped gate electrode region of the plurality of loop-shaped gate electrode regions are disposed onto two positions between the source regions and the drain regions.

10. **Claims 1-2 and 4-7** are rejected under 35 U.S.C. 102(b) as being anticipated by Shimomura et al. U.S. Patent 6,140,687 (the '687 reference).

The '687 reference discloses in the figures, particularly in Figs. 7-8, and respective portions of the specification a semiconductor device as claimed.

Referring to **claim 1**, the reference discloses a semiconductor device, comprising:

a first transistor (such as the left transistor in Figs. 8-9, which transistor generally defined by source 3, drain 2, and gate 1, column 16, lines 19+, column 12, lines 19+) including a source region (3), a drain region (2) provided in the same device region as the source region, and a loop-shaped gate electrode region (1, Figs. 1, 7-8, best seen in Fig. 1); and

a second transistor (such as the right transistor in Figs. 8-9, which transistor generally defined by source 3, drain 2, and gate 1) sharing, with the first transistor, the loop-shaped gate electrode region (1) and (the source region or) the drain region (2).

Referring to **claim 2** and using the same reference characters, citations, and interpretations as detailed above for claim 1 where applicable, the reference discloses a semiconductor device, comprising:

a device region where each of a plurality of source regions (3) and each of a plurality of drain regions (2) of transistors are alternately included; and

a plurality of loop-shaped gate electrode regions (1) of the transistors which are formed on the device region and portions of each loop-shaped gate electrode region of the plurality of loop-shaped gate electrode regions are disposed onto two positions between the source regions and the drain regions (best visualized in Figs. 7-8).

Referring to **claim 4**, the reference further discloses that the drain region (2) is formed in a region surrounded by the loop-shaped gate electrode region (1, best seen in Fig. 1).

Referring to **claim 5**, the reference further discloses that an electrically independent drain region (2) is formed in a region surrounded by the loop-shaped electrode region.

Referring to **claim 6**, the reference further discloses that the source region (3) is formed outside a region surrounded by the loop-shaped gate electrode region (1, best seen in Fig. 1).

Referring to **claim 7**, the reference further discloses that a plurality of the source regions (3) are formed outside a region surrounded by the loop-shaped gate electrode region (1), the plurality of the source regions electrically coupled to each other (through wire 15, not shown in Fig. 7, column 16, lines 20-30).

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 6:30 am - 5:00 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TH

Tu-Tu Ho
November 06, 2005